HEWLETT PACKARD

Breadboard Interface

Technical Data

For HP 1000
A-Series Computer Systems
Product Number
12010A

The HP 12010A Breadboard Interface provides the standard A-Series I/O master circuit along with space for sixty 16-pin wire wrap sockets for user-designed custom interfaces. The printed circuit layout is based on a 2.5 mm (0.1 in) by 7.6 mm (0.3 in) matrix, which accommodates any mix of dual or single in-line integrated circuits. All signals needed by the user are brought along with dc power supply voltages to convenient, labeled connection pads along the edge of the I/O master circuit area.

Features

- Standard A-Series I/O master interface to computer or system backplane
- Built-in DMA capability for optimum I/O efficiency
- 60-socket space for user's circuits
- TTL-compatible signals

Functional Specifications

I/O Master

Purpose: To ensure compatibility of user-designed interfaces with the high performance I/O design of A-Series Computers and Systems, the Breadboard Interface includes the same I/O master circuit as other A-Series interfaces. This includes the CMOS LSI I/O Processor chip, which executes I/O instructions, and other circuits that make high-speed transfers possible.

Determination of I/O Address: I/O address select code is set by select code switches and is independent of interface card position along the A-Series backplane bus.

I/O Addressing: The Breadboard Interface may be preaddressed by presetting the select code into its Global Register (GR), which leaves the six select code bits of I/O instructions available for addressing registers or other functions on the interface. Alternatively, the GR can be turned off and the select code bits in each instruction can be used to address the user-designed custom interface.

I/O Device Interrupt Priority: Depends upon I/O interface position in the cardcage with respect to the processor board.

Interrupt Masking: Under program control an interrupt mask register provides selective inhibition of interrupts from specific under program control. This capability can be programmed interfaces to temporarily cut off undesirable interrupts from any combination of interfaces when they could interfere with crucial transfers.

Direct Memory Access (DMA): The I/O master supports DMA capability for user's circuits on the breadboard interface. This feature reduces the number of interrupts from one per data item (byte or word) to one per complete DMA block transfer, greatly reducing overhead and increasing throughput.

Self-Configured, Chained DMA: A self-configuring mode of DMA operation is available for when groups of DMA transfers must be performed. In this mode, instead of interrupting after a block transfer, the I/O master fetches a new set of DMA control words for the next transfer, reconfigures itself, and initiates another block transfer. This chained process continues as long as additional control word sets are available.

Data Packing under DMA: When byte mode is specified in control word instructions, the I/O master automatically manages byte packing or unpacking.

Maximum Achievable DMA Rate: 700,000 words/second (1.4 Mbytes/second)

Virtual Control Panel Support: The I/O master supports the provision of virtual control panel interface capability on user-designed custom interfaces based on the breadboard interface.

I/O Master Signals and Timing: Refer to the HP 1000 A-Series I/O Interfacing Guide (02103-90005)

User's Circuit Space

Area: 13.3 cm by 14.6 cm (5.25 in by 5.75 in)

Organization: The user's circuit area is organized into ten column pairs of 53 circuit pads each for mounting up to sixty 16-pin wire-wrap integrated circuit sockets or any other combination of dual in-line integrated circuit sockets with different numbers of pins.

Maximum Component Height above board surface: 10mm (0.4 in) for an interface capable of being installed in any circuit card position in the 12030A or 2103L 10-slot cardcage, 12032A 5-slot cardcage, or 2145B 16-slot cardcage. Height can be up to 1.8cm (0.7 in) for an interface to be used only in 10-slot cardcage slot XA6 or 16-slot cardcage slot XA9

Maximum Permissible Depth below board for leads or attaching hardware: 5 mm (0.2 in)

Power Dissipation

Maximum per A-Series Interface Card: 17 W, determined by air flow provided through the cardcages

I/O Master Dissipation: 5.29 W

Power Dissipation Capacity available for user's circuits: 11.7 W

Configuration Information

Computer and System Compatibility: The I/O master on the HP 12010A Breadboard Interface is compatible with all HP 1000 A-Series Computers and Systems.

Software Support: User's custom-designed interfaces based on the HP 12010A Breadboard Interface will require user-written RTE-A/L driver software, which can be modeled on the general-purpose RTE-A/L driver ID.50.

Diagnostic Support: Diagnostic support for user's custom-designed interfaces must be user written. A kernel diagnostic, supplemented by a BASIC-like interactive diagnostic test and design language is provided in the HP 24612A Diagnostic Package to assist the user's diagnostic development efforts.

Installation: Build user's custom interface on the breadboard interface; establish control settings as required for the user's custom applications; set select code switches to the appropriate I/O address; turn off power to the computer and the interfaced device; plug the custom interface into the computer backplane; connect an appropriate cable, and integrate the interface and its user-written driver into the RTE- A/L operating system.

Note: The I/O address setting of the interface select code switches is independent of the interface card's position in the computer backplane.

Electrical Specifications

Direct Current Requirements: The I/O master requires 0.912A (+5 V), and 0.061A (+12 V).

Physical Characteristics

Dimensions: 28.9 cm long by 17.2 cm wide by 0.21 cm board thickness (11.38 in by 6.75 in by 0.063 in), with 1.0 cm (0.4 in) top-of-board parts clearance and 0.5 cm (0.2 in) beneath-board clearance.

Weight: 313 grams (11 oz) with mating connector

Power Sources Available:

dc/ac Voltages	P2 Pin(s)
+5.0 V dc	35-37
+12.0 V dc	41, 42
-12.0 V dc	43, 44
19.5 V ms, 25kHz*	47, 48
common	2, 15, 17, 21, 27, 34
19.5 V ms, 25 kHz*	49, 50

* The 19.5 V ms, 25 kHz power is available for metting unique power supply requirements. For more information, see HP Application Note 404-3, which is available from your HP Representative.

Ordering Information

The HP 12010A includes:

12010-60003 Breadboard Interface Card
5061-3426 8-pin Connector Kit
02103-90005 A-Series I/O Interfacing Guide